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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,905	WALACAVAGE ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10 and 12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10 and 12-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/30/06, 9/18/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-8, 10, and 12-21 were rejected in the Office Action of 14 February 2006. Applicants' response of 18 May 2006 has amended claims 1, 3-5, 12, 15, 16, and 21. Claims 1-8, 10, and 12-21 are pending in this application

Claims 1-8, 10, and 12-21 are rejected.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 30 May 2006 was filed after the mailing date of the Office Action on 14 February 2006. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

2. The information disclosure statement (IDS) submitted on 18 September 2006 was filed after the mailing date of the Office Action on 14 February 2006. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8, 10, and 12-21 are rejected under 35 U.S.C. § 102(b) as being anticipated by "Emulation of a Material Delivery System" by Todd LeBaron and Kelly Thompson (LeBaron).

Regarding claims 1, 10, 12, 20, and 21, LeBaron discloses:

A computer-implemented method for verification of part flow in a system [*"Emulation of the complex pick and pack conveyor system will be presented."* (page 1055, left column, Abstract); *"The material handling system consists of conveyor sections which continuously move carriers around a closed loop that connects all pick and pack stations."* (page 1055, left column, System Description)] including a programmable logic controller verification [*"Routing logic, PLC or PC control software, sequencing algorithms, and more can be integrated, tested, and debugged within a simulation environment."* (Henceforth "control logic" refers to at least controller logic in a PLC.) (page 1055, left column, Abstract); *Emulation has been used for a Rapistan Systems project to test, debug, and optimize complex algorithms and control logic."* (page 1055, left column, Abstract)], comprising the steps of:

Constructing a simulation model of a part flow in a manufacturing line using a computer [*"The material handling system consists of conveyor sections which continuously move carriers around a closed loop that connects all pick and pack stations."* (A part flow in a manufacturing line.) (page 1055, left column, System Description); *"Emulation of the complex pick and pack conveyor system will be presented."* (page 1055, left column, Abstract)];

Representing a part and part locations of the manufacturing line [*"A graphical representation of the pick and pack conveyor system is shown in Figure 1."* (page 1055, left column, System Description); (Figure 1, page 1056)];

Playing the simulation model by a PLC logical verification system on the computer [*"Emulation of the Rapistan control system for this project integrates a simulation model with the actual control system. The simulation model provides the output for evaluating control logic and algorithms."* (page 1055, right column, Emulation); *"The simulation model provides the output for evaluating control logic and algorithms. The simulation model also provides real time 3-D graphical animation for improved visibility and confidence."* (page 1055, right column, Emulation)];

And allowing a user to visually see flow of a part through the manufacturing line [LeBaron discloses a "Simulation Model: Graphical Animation" (page 1056, Figure 2) and *"The simulation model also provides real time 3-D graphical animation for improved visibility and confidence."* (page 1055, right column, Emulation). Further, LeBaron does not disclose *prohibiting* a user from visually seeing flow of a part through the manufacturing line, and therefore anticipates the claim language that *allows* this feature.];

Determining if the part flow represented in the simulation model is correct [*"The emulation used at Rapistan Systems was able to prove that the system could handle the projected growth in daily orders."* (page 1060, left column, Summary)];

Modifying the part flow represented in the simulation model if the part flow represented in the simulation model is not correct [*"RULE1 was developed to improve the FIFO algorithm."*, (page 1058, right column, The RULE1 Algorithm)]; and

Using the part flow simulation model to test PLC code [*"Emulation provides the graphical and statistical output needed to accurately evaluate different algorithms and control logic."* (page 1060, left column, Summary)] and implementing the manufacturing line according to the part flow simulation model [*"Because the actual control system is used to develop, test, and refine algorithms and logic, it exists as developed in the real system. This eliminates re-implementation errors and provides greater confidence in the emulation results.* (page 1055, left column, Abstract); *"during the refinement process, two initial algorithms were developed and compared. These two algorithms are called the FIFO and RULE1."* (page 1057, right column, Algorithm Development); *"The emulation results indicate that using the correct order scheduling and pack assignment algorithm is key to improving pack station utilization and system throughput."* (page 1060, left column, Analysis)].

In response, Applicants argue primarily that:

> In LeBaron et al., there is no PLC logical verification system and no PLC code is generated. The PLC logical verification system is not an emulator.

The Examiner respectfully traverses this argument as follows.

In LeBaron, the emulator is employed to verify the PLC logic. Therefore, the emulator is a PLC logical verification system. Further, Applicants' arguments suggest what the PLC logical verification system is not, but have not explained what it is. The Examiner respectfully suggests that Applicants show specific intrinsic or extrinsic evidence to define a PLC logical verification system. Should that specific evidence clearly distinguish a "PLC logical verification system" from an "emulator," that evidence may be found persuasive in overcoming the LeBaron reference.

Additionally, the Examiner traversed a similar argument in the previous Office Action by stating:

> Thus the entire computer system is regarded as a "PLC logical verification system on a computer." LeBaron expressly discloses that the "PLC or PC control software" "can be ... tested, and debugged within a simulation environment." In the Examiner's interpretation, LeBaron thus discloses a "PLC logical verification system on a computer." If Applicants' regard the term "PLC logical verification system" to hold a separate specific definition, the Examiner respectfully suggests claim language which recites that definition. (Office Action, 14 February 2006, page 5)

Applicants have not provided a specific definition for the term "PLC logical verification system."

Applicants further argue that:

> LeBaron et al. also lacks using the generated PLC code and implementing the manufacturing line according to the part flow simulation model.

The Examiner respectfully traverses this argument as follows.

LeBaron expressly discloses this limitation [*"One of the main benefits of emulation is that it eliminates the need to re-implement code. Because the actual control system is used to develop, test, and refine algorithms and logic, it exists as developed in the real system."* (page 1055, left column, Abstract); *"The emulation used at Rapistan Systems was able to prove that the system could handle the projected growth in daily orders. In addition, emulation provided the tool to refine the scheduling logic used by the control system, providing great confidence that the system could meet the daily order requirements."* (page 1060, left column, Summary); et seq.]. That is, LeBaron is specifically concerned with implementing the generated PLC code in the manufacturing line according to the part flow simulation model. Implementing the control logic and algorithms in the actual system is the impetus for the majority of the LeBaron reference

[For example, *"By developing and refining the control logic and algorithms in the control software, it exists as developed."* (page 1055, right column, Emulation)].

Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claims 2-5 and 13-16, LeBaron discloses selecting a part generator, generating a part with the part generator, and identifying part locations of the generated part within the manufacturing line [*"Emulation of the complex pick and pack conveyor system will be presented."* (page 1055, left column, Abstract); *"All of the components for a particular order are assigned and routed to a specific pack station."* (page 1055, right column, System Description); The analysis is conducted for a simulated 23-hour period (page 1060, left column, Analysis) which implicitly discloses the generation of components for a particular order so that the emulation can fulfill the order.].

Regarding "testing the generated part at the part location", the specification teaches this limitation as determining if the part is present or not present (specification as amended, page 12, lines 9-11). LeBaron discloses emulation of a pick and pack conveyor system and therefore implicitly discloses "testing the generated part at the part location" as the ability to detect if the part is present or not present is a basic underlying principle in the proper operation of a pick and pack conveyor system. Further emphasis of this is LeBaron's disclosure [*"The goal in developing algorithms was to process the required number of orders per day within the planned facility schedule. Fully utilizing the pack stations is key in accomplishing this goal."* (page 1057,

right column, Problem Description)] that clearly implies that pack stations can determine whether a necessary generated part is present at that pack station.

Regarding claims 6-8 and 17-19, LeBaron discloses constructing records for the parts [*orders*] wherein the record has at least one resource and at least one capability [*"Historical data was used to generate daily order profiles (as in Table 1)."* (page 1057, right column, Problem Description); Table 1 shows records [*orders*] for the parts, including a resource [*Pick Station*] and a capability [*# Pick Types*]].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR)

system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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11/30/06